ABSTRACT OF THE DISCLOSURE

A processor may include an execution circuit, an issue circuit coupled to the execution circuit, and a clock tree for clocking circuitry in the processor. The issue circuit issues an instruction to the execution circuit, and generates a control signal responsive to whether or not the instruction is issued to the execution circuit. The execution circuit includes at least a first subcircuit and a second subcircuit. A portion of the clock tree supplies a plurality of clocks to the execution circuit, including at least a first clock clocking the first subcircuit and at least a second clock clocking the second subcircuit. The portion of the clock tree is coupled to receive the control signal for collectively conditionally gating the plurality of clock, and is also configured to individually conditionally gate at least some of the plurality of clocks responsive to activity in the respective subcircuits of the execution circuit. A system on a chip may include several processors, and one or more of the processors may be conditionally clocked at the processor level.